Fully Differential Direct Conversion Receiver for W-CDMA using an Active Harmonic Mixer

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Abstract — **A fully differential direct conversion receiver IC for W-CDMA is presented. The receiver IC consists of a complete active portion of a W-CDMA receiving system, such as an LNA, quadrature demodulator, low-pass filter (LPF), and variable gain amplifier (VGA). In order to suppress the DC offset, which is the most important issue in a direct conversion system, an active harmonic mixer is applied to the quadrature demodulator. Furthermore, the receiving system, including an LNA and RF filter, adopts a differential architecture to reduce local signal leakage, which generates DC offset. The performance of the entire receiving system was evaluated and the DC offset in steady state was measured at only 40 mV. Moreover, the DC offset variation in the LNA gain change, which has the largest affect on the receiving performance, was limited to 60 mV, which is less than –10 dB compared to the desired signal strength. It was confirmed by computer simulation that the DC offset variation in the LNA gain change did not degrade the bit error rate (BER) performance at all.**

I. Introduction

W-CDMA, the 3rd generation cellular phone system, is now in practical use. As with conventional cellular phones, there is a need for reductions in the size and cost of W-CDMA handsets. In comparison to a conventional super-heterodyne system, a direct conversion receiver system requires no large or bulky external components such as an IF filter, and is therefore suitable for creating small, low-cost radio terminals. Hence, some direct conversion receiver ICs for W-CDMA have been reported [1][2]. However, direct conversion receiver systems have an essential problem in which the DC offset resulting from local leakage or the second-order distortion of a quadrature demodulator significantly degrades the receiver performance [3]. In order to suppress the DC offset, a harmonic mixer for the quadrature demodulator can be effectively used [4][5]. This paper introduces a fully integrated direct conversion receiver IC for W-CDMA, in which an active harmonic mixer is applied to a quadrature demodulator, and a fully differential architecture is introduced for the receiver chain. In addition, evaluation results are presented for a receiver system using a direct conversion IC, in which the DC offset is significantly reduced.

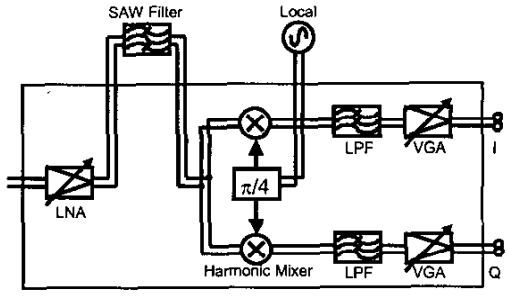

Fig. 1. Configuration of Receiver Chain

II. Configuration of The Receiver Chain Including The Direct Conversion IC

The configuration of the receiver is shown in Fig. 1. The receiver IC consists of the LNA, quadrature demodulator, channel-selection LPF, and VGA. The output of the LNA is inputted into a quadrature demodulator through the external SAW filter, which suppresses the transmitted signal. The active harmonic mixer is adopted for the quadrature demodulator in order to reduce the DC offset.

Unlike a conventional mixer, half of the received frequency is required for the harmonic mixer. Therefore, the DC offset caused by self-mixing is not inherently generated because the local frequency is different from the received frequency. However, the leakage of the local signal to the RF input port generates DC offset even if the mixer itself does not produce DC offset due to self-mixing, because second-order harmonics whose frequency is identical to the received frequency are contained in the local VCO (Fig. 2).

The influence of local leakage to the RF input port is most remarkable in the case where the LNA gain changes. If the leakage level to the RF input port from the VCO is

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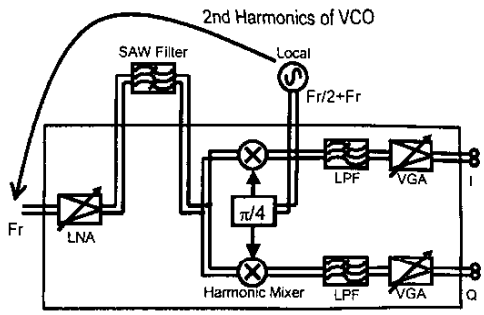

Fig.2. Local Leakage to LNA Input Port

fixed, the DC offset caused by local leakage remains a constant voltage. This constant DC offset can be eliminated by means of DC offset canceling, such as AC coupling or a DC offset canceler. However, in cases in which there are discrete LNA gain changes of, for example, 30 dB, the local leakage level through the LNA to the quadrature demodulator changes significantly. At this time, the DC offset varies with the transient response of the DC offset canceling mean, which generally has a high-pass filtering characteristic, and the receiving performance is significantly degraded. In order to overcome this problem, a fully differential configuration, which uses a differential LNA and RF filter to reduce the leakage to the LNA input port from the VCO, was introduced.

As mentioned above, the direct conversion receiver system, in which a dynamic variation of DC offset is suppressed to the minimum voltage, is realized by utilizing an active harmonic mixer for the quadrature demodulator and applying a fully differential architecture.

II. Receiver IC Architecture

Each circuit block that forms the receiver IC is explained below.

The LNA has a differential input port and a differential output port in order to reduce the leakage of the local signal as described in the previous section. The output matching circuit is built in the IC and no external components are needed. The LNA has a gain change function with 32 dB increments. The LNA output is connected to an external SAW filter with a differential input port.

A quadrature demodulator subsequent to the external SAW filter adopts the active harmonic mixer in order to suppress the DC offset. The local frequency is half of the received frequency.

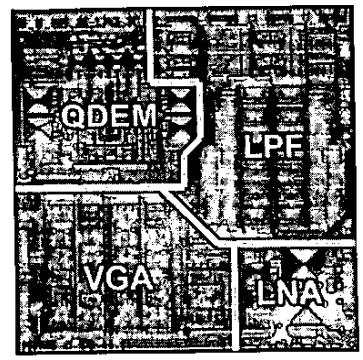

Fig. 3. Die Photograph of W-CDMA Receiver IC

LPFs with a corner frequency of 1.92 MHz consist of 8th-order filters. With these filters, the desired signal is channel-selected and interference such as adjacent channel signals and blockers are eliminated.

The VGAs have a gain variable function of more than 60 dB, and contain DC offset cancelers to remove the DC offset generated in the quadrature demodulator and the LPFs. The corner frequency of the DC offset canceler remains constant around 10 kHz. Detailed descriptions of the LPFs and VGAs are provided in [6] and [7], respectively.

A die photograph of the receiver IC is shown in Fig. 3. The manufacturing process was SiGe-BiCMOS with 35 GHz f_T. The chip area is 3.6 mm x 3.6 mm.

III. Measurement Results

The performance of the receiver chain was evaluated on an evaluation PCB, on which the receiver IC, SAW filter, and external matching circuit were mounted.

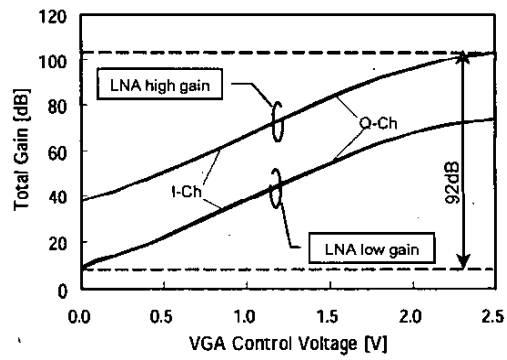

Fig. 4. Total Gain of Receiver Chain

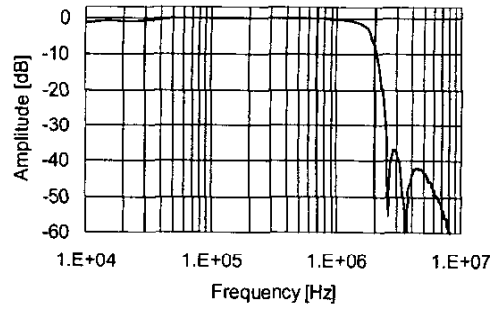

Fig. 5. Frequency Characteristic in Baseband

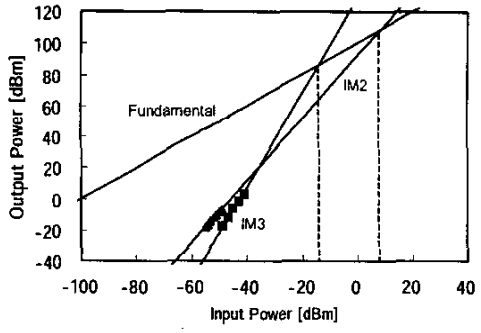

Fig. 6. Measured IIP2 and IIP3

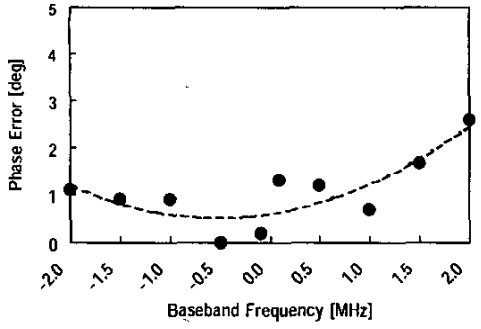

Fig. 7. Phase Error of Total Receiver Chain

A. Total Gain

The total gain in the receiver chain in respect of the VGA control voltage is shown in Fig. 4. As shown in the figure, more than 92 dB of dynamic range was achieved with the LNA gain change function. Furthermore, less than 0.5 dB of amplitude error in the IQ channel was obtained.

B. Frequency Characteristic in Baseband

The frequency characteristic from the LNA input to the VGA output is shown in Fig. 5. An adjacent channel rejection ratio of 37 dB at 5 MHz offset was achieved.

C. Cascaded Noise Figure (NF)

The NF of the cascaded receiving system from LNA input to VGA output was 5.8 dB in the 98 dB total gain setting.

D. IIP2 and IIP3

The measurement results for IIP2 and IIP3 are shown in Fig. 6. These results indicate that IIP2 and IIP3 of 8.2 dBm and –13.9 dBm were obtained, respectively.

E. Phase Error

The phase error measurement result is shown in Fig. 7. A phase error in baseband of less than 2.6 degrees within +/– 2 MHz was achieved.

F. DC Offset

The DC Offset in steady state was less than 40 mV in the maximum gain setting. The dynamic variation of the DC offset was less than 60 mV. The dynamic variation of the DC offset is described in detail in the following section.

The measurement results of the cascaded receiving system are shown in Table I. These measurement results show that the 3GPP specification can be satisfied by the receiver IC.

Table I. Cascaded Receiver Measurement Results

NF	5.8 dB
IIP2	8.2 dBm
IIP3	–13.9 dBm
Maximum Voltage Gain	102 dB
Minimum Voltage Gain	10 dB
Total Gain Control Range	92 dB
Adjacent Channel Rejection Ratio	37 dBc
DC Offset (steady state)	40 mV
DC Offset (dynamic variation)	60 mV
Phase Error	2.6 deg
Amplitude Error	0.5 dB
Power Consumption	52.7 mA
Power Supply Voltage	2.9 V
Chip Area	3.6 mm x 3.6 mm

IV. System Simulation of BER Performance

The DC offset is transitionally varied by the high-path characteristic of the DC offset canceler included in the VGAs in the gain change of the receiver chain. This variation is most remarkable in the case where the LNA gain is reduced. The measurement results for the DC offset variation in this case are shown in Fig. 8. This DC offset variation originates in the local signal leakage, and the sum total of the DC offset generated in QDEM, LPF, and VGA itself. As shown in the figure, a peak voltage of the DC offset transition of 50 mV for I-channel and 60 mV for Q-channel was observed, respectively.

In order to evaluate the performance degradation for the receiver chain caused by this DC offset variation, the bit error rate (BER) performance was computer simulated under the conditions of the 3GPP standard [8] as shown in table II. The simulation results for BER performance with respect to Eb/N_0 is shown in Fig. 9. These simulation results indicate that no degradation of BER performance with DC offset variation in the LNA gain change was observed.

TABLE II. Simulation Condition

DPCH/Ior	-10.3 dB
Ior/Ioc	4 - 0 dB
Spreading Factor	128
AGC Target Voltage	164 mVrms
Gain Change Interval	2 msec

V. Conclusion

A receiver IC for W-CDMA was fabricated using a direct conversion architecture. The DC offset was suppressed by adopting an active harmonic mixer for the quadrature demodulator and introducing a fully differential construction for the receiver chain. The measurement results indicate that the receiver IC satisfies the 3GPP specifications. Furthermore, the computer simulation results for the BER performance indicate that the DC offset variation in the LNA gain change does not degrade the BER performance of the receiver system. These performance results indicate that a direct conversion receiver system for the receiver IC can be used for W-CDMA.

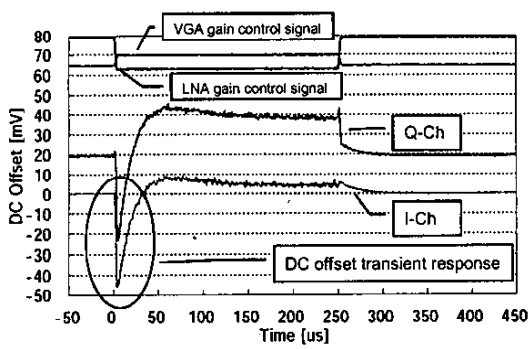

Fig. 8. Dynamic variation of DC offset

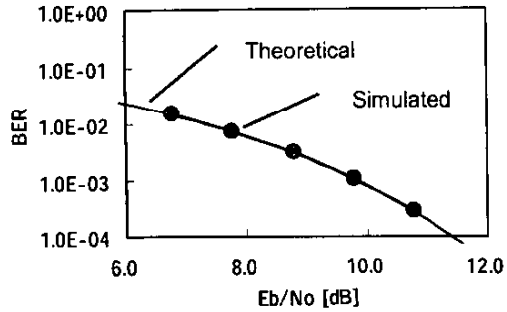

Fig. 9. Simulation result of BER performance

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